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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/654,527	09/01/2000	Hideo Miyake	1614.1074	7021

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EXAMINER
HARKNESS, CHARLES A

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/654,527	MIYAKE ET AL.	
	Examiner	Art Unit	
	Charles A Harkness	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. In view of Applicant's amendment to the title, the previous objection has been withdrawn.

2. In view of Applicant's amendment to the claims, the previous objection has been withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Faraboschi et al, U.S. Patent Number 5,930,508 (herein referred to as Faraboschi).

4. Referring to claims 1 and 12 Faraboschi has taught a parallel processor performing parallel processing of one or more basic instructions contained in each of a plurality of instruction words delimited by instruction delimiting information, said parallel processor comprising (Faraboschi figures 4 and 5 abstract column 3 lines 16-25):

A plurality of instruction execution units performing processes in accordance with corresponding, supplied basic instructions in parallel (Faraboschi figure 1 abstract column 3 lines 16-20 column 4 lines 46-48);

An instruction fetch unit fetching the instruction words one by one in accordance with the instruction delimiting information (Faraboschi figure 7 column 3 lines 16-25 column 7 lines 32-36; the alignment logic 720 acts as the fetch unit); and

An instruction issue unit recognizing and, in accordance therewith, selectively each of the basic instructions supplied from the instruction fetch unit to one of the corresponding instruction execution units to execute the issued basic instruction (Faraboschi column 3 lines 25-32, column 4 line 57-column 5 line 11).

5. Referring to claim 2 Faraboschi has taught wherein the plurality of instruction execution units all have the same structure (Faraboschi column 4 lines 46-50; the execution units may include two or more arithmetic units for parallel computation, and it would be inherent that the arithmetic units would perform the same functions, and does not necessarily include the multipliers since it is stated as the arithmetic units and/or multipliers).

6. Referring to claim 3 Faraboschi has taught wherein at least two of the instruction execution units have different structures from each other (Faraboschi column 4 lines 46-53; the execution units include some arithmetic units and some multipliers); and

The instruction fetch unit rearranges the basic instructions contained in each of the fetched instruction words, in accordance with arrangement of the plurality of instruction execution units (Faraboschi figures 6 and 7, column 3 lines 20-25 and column 4 line 57-column 5 line 25 column 5 lines 52-60 and column 7 lines 32-44; figure 6 is represented in figure 7 by block 720, which is the alignment means, or logic, and has the same functionality as the fetch unit as described by applicant), and then supplies the rearranged basic instructions to the instruction issue unit (Faraboschi column 3 lines 23-32 and column 7 lines 37-44).

7. Referring to claim 4 Faraboschi has taught wherein at least two of the instruction execution units have different structures from each other (Faraboschi column 4 lines 46-53; the execution units include some arithmetic units and some multipliers); and

The instruction issue unit rearranges the basic instructions contained in each of the instruction words supplied from the instruction fetch unit, in accordance with arrangement of the plurality of instruction execution units, and then supplies the rearranged basic instructions to the instruction execution units (Faraboschi figure 4 reference number 740 and column 7 lines 37-44; the expansion block 740 acts as the issue unit as described by applicant).

8. Referring to claim 5 Faraboschi has taught wherein at least two of the instruction execution units have different structures from each other (Faraboschi column 4 lines 46-53; the execution units include some arithmetic units and some multipliers); and

The instruction fetch unit rearranges the basic instructions contained in each of the fetched instruction words, in accordance with arrangement of the instruction execution units (Faraboschi figures 6 and 7, column 3 lines 20-25 and column 4 line 57-column 5 line 25 column 5 lines 52-60 and column 7 lines 32-44; figure 6 is represented in figure 7 by block 720, which is the alignment means, or logic, and has the same functionality as the fetch unit as described by applicant), and then supplies the rearranged basic instructions to the instruction issue unit (Faraboschi column 3 lines 23-32 and column 7 lines 37-44); and

The instruction issue unit further rearranges the basic instructions contained in each of the instruction word supplied from the instruction fetch unit, in accordance with the arrangement of the instruction execution units, and then supplies the rearranged basic instructions to the instruction execution units (Faraboschi figure 4 reference number 740 and column 7 lines 37-44; the expansion block 740 acts as the issue unit as described by applicant).

9. Referring to claim 6 Faraboschi has taught wherein at least two of the instruction execution units have different structures from each other (Faraboschi column 4 lines 46-53; the execution units include some arithmetic units and some multipliers); and

The instruction fetch unit fetches an instruction word that contains basic instruction arranged in advance in accordance with the arrangement of the instruction execution units (Faraboschi column 4 line 57-column 5 line 25; since the different syllables S1, S3, etc. already have the dispersal bit sets that include the functional unit where the syllable is to be executed, they are already aligned, or arranged in accordance with the execution units).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faraboschi in view of Nair et al, "Exploiting Instruction Level Parallelism in Processors by Caching Scheduled Groups" (herein referred to as Nair).

11. Referring to claim 7 Faraboschi has not explicitly taught wherein, depending on the type of basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues a next basic instruction before the execution of the basic instruction being currently executed is completed. However, Faraboschi has taught using different execution units to perform different functions (Faraboschi column 4 lines 46-53; arithmetic units and multipliers). Therefore, issuing the basic instruction to an execution unit is dependent on the type

of basic instruction that is performed by the execution unit. Also Faraboschi taught a buffer to hold the basic instructions awaiting the execution unit (Faraboschi figure 7 reference number 750), where the buffer holds the basic instructions issued by the processor before the execution is completed with the current instruction. Nair has taught has taught wherein, depending on the type of basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues a next basic instruction before the execution of a basic instruction being currently executed is completed (Nair page 18 column 2 line 2-page 19 column 2 line 1; Nair teaches that each functional unit performs only a subset of all operations performed by the processor; Nair also teaches that scheduling instructions basically involves examination of resources needed by each instruction, so that if some resources are available to begin execution on the next instruction if those are the resources required by the next instruction, even if the previous instruction is still executing; this goes along with the teaching of the Applicant on pages 12-13 from which claim 7 is assumed to have originated from). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Nair with the teachings of Faraboschi to issue instructions based on the type of instruction before a previous instruction is done executing. Issuing instructions before the previous instruction is completed is known as pipelining, or sometimes micro- pipelining, and increases throughput of the execution units since the instructions do not have to wait for the previous instruction to completely finish before starting execution. Also, by having certain execution units perform a subset of all the functions of the processor, the plurality of execution units take up less space, since it does not require all of the functionalities to perform all of the functions of the processor (Nair page 18 column 2 paragraph 1-2). Therefore, it would have been obvious to one of

ordinary skill in the art at the time of the invention to issue an instruction to a execution unit designated for certain operations, and to issue instructions before the previous instruction is completed to decrease complexity of the execution units to save production costs, and to increase throughput which reduces execution time, respectively.

12. Referring to claim 8 the combination of Faraboschi and Nair has taught wherein, if a supplied basic instruction does not have data dependency or control dependency, or does not share resources with a basic instruction being currently executed by one of the instruction execution units, the instruction issue unit issues the supplied basic instruction before the execution of the basic instruction being currently executed is completed (Nair page 19 column 2 lines 1-8; Nair teaches that if an instruction is dependent on data currently being executed, that is not issued, but if it is not dependent on the instructions currently being executed, then the instruction is issued).

13. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Faraboschi in view of Park et al, U.S. Patent Number 5,881,307 (herein referred to as Park).

14. Referring to claim 9 Faraboschi has not explicitly taught wherein the instruction issue unit further comprises an interface corresponding to the instruction execution units indicating whether the corresponding instruction execution unit is available. Park has explicitly taught wherein the instruction issue unit further comprises an interface corresponding to the instruction execution units indicating whether the corresponding instruction execution unit is available (Park column 5 lines 36-54). It would have been obvious to one of ordinary skill in the art at the time of the invention looking at Faraboschi to recognize that some interface would be required between the issue unit, or the buffers holding the instructions, to indicate that the functional units

were ready for the next instruction. If the functional units required were not available, or were not ready, for the next instruction, then issuing the next instruction would cause errors in the system. Looking at figure 7 of Faraboschi, one can see that there is a buffer leading into the functional unit. It is obvious that some unit or piece of logic could be used to indicate when to send the next instruction, which is shown by Park. Since Faraboschi lacks the details of when the issuing unit should know exactly when to send the instruction, one of ordinary skill in the art at the time of the invention would have looked to Park for the missing details. Park teaches a resource scoreboard, which indicates if a resource is ready for an instruction. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have an interface for indicating if a functional unit is available to prevent errors that would occur from an issuing unit sending an instruction to a functional unit before it has completed execution on a previous instruction.

15 Referring to claim 10 the combination of Faraboschi and Park has taught wherein the instruction issue unit further comprises a table for setting effective bits to indicate availability of the corresponding instruction execution unit (Park column 5 lines 36-54; the scoreboard as taught by Park would indicate the available resources by some bits, since in digital processing, which all of the reference used pertain to, bits are used to indicate information and data through binary logic).

16. Referring to claim 11 the combination of Faraboschi and Park has taught wherein a first instruction word format is converted into a second instruction word format by the table, the first instruction word format indicating an arrangement of the instruction words from the instruction fetch unit, and the second instruction word format indicating an arrangement of instruction words

which corresponds to the instruction execution units (Faraboschi Figure 4, column 4 line 57-column 5 line 18).

17. Referring to claim 12 the combination of Faraboschi and Park has taught wherein the instruction issue unit further comprises a conversion unit for converting a first instruction word format into a second instruction word format on the basis of effective bits, corresponding to the instruction execution units, indicating whether the corresponding instruction execution unit is available (Faraboschi Figure 4, column 4 line 57-column 5 line 18).

18. Referring to claim 13 the combination of Faraboschi and Park has taught wherein the first instruction word format indicates an arrangement of instruction words from the instruction fetch unit, and the second instruction word format indicates an arrangement of instruction words which corresponds to the instruction execution units (Faraboschi Figure 4, column 4 line 57-column 5 line 18).

19. The rejection of the claims are respectfully maintained and incorporated by reference as set forth in the last Office Action, mailed 02/12/03, paper number 5.

Response to Arguments

20. Applicant's arguments filed 06/16/03, paper number 7, have been fully considered but they are not persuasive.

21. In the remarks, in regard to the rejection of claim 1, Applicant argues in essence that:

"This is in contrast with the present invention, which provides the processor with flags, corresponding to respective, individual execution units in the processor...these flags are not attached to the basic instructions, as are the dispersal bits in Faraboschi ..."

22. This is not found persuasive. Applicant is arguing a feature of the invention not specifically stated in the claim language, which is improper. Claimed subject matter, not the

specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Self*, 213 USPQ 1,5(CCPA 1982); *In re Priest*, 199 USPQ 11,15 (CCPA 1978). Nowhere in the independent claims is any mention of flags which correspond to execution units, or that these flags are not attached to the basic instructions.

23. In the remarks, in regard to the rejection of claim 1, Applicant argues in essence that:

"This allows the instruction codes to be stored in a memory device with only delimiter data, as opposed to each instruction having a dispersal bit attached along with delimiter data."

24. This is not found persuasive. The dispersal bits as taught by Faraboschi are in addition to the elements claimed by Applicant, and Applicant does not claim that such elements are not present, so the argument that the Applicant's invention does not contain dispersal bits in memory whereas Faraboschi does, is not persuasive. According to MPEP § 2111.03, the transitional term "comprising", which is synonymous with "including," "containing," or "characterized by," is inclusive or open-ended and does not exclude additional, unrecited elements or method steps. See, e.g., Genentech, Inc. v. Chiron Corp., 112 F.3d 495, 501, 42 USPQ2d 1608, 1613 (Fed. Cir. 1997) ("Comprising" is a term of art used in claim language which means that the named elements are essential, but other elements may be added and still form a construct within the scope of the claim.); Moleculon Research Corp. v. CBS, Inc., 793 F.2d 1261, 229 USPQ 805 (Fed. Cir. 1986); In re Baxter, 656 F.2d 679, 686, 210 USPQ 795, 803 (CCPA 1981); Ex parte Davis, 80 USPQ 448, 450 (Bd. App. 1948) ("comprising" leaves "the claim open for the inclusion of unspecified ingredients even in major amounts").

25. In the remarks, in regard to the rejection of claim 1, Applicant argues in essence that:

"Referring to claim 1 as amended, its is submitted that Faraboschi does not teach...having an instruction issue unit that 'includes an interface having effective bits corresponding to the instruction execution units, the effective bits indicating whether the corresponding instruction execution unit is available.'"

26. This is not found persuasive. The above-cited limitations are absent from the claims 1 and 14, therefore rendering these arguments non-persuasive. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Self*, 213 USPQ 1,5(CCPA 1982); *In re Priest*, 199 USPQ 11,15 (CCPA 1978).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness
Examiner
Art Unit 2183
August 14, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100